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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/748,509	12/26/2000	Koji Hayashi	10449-030001	4131

26161 7590 08/04/2004

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EXAMINER	
CHU, KIM KWOK	
ART UNIT	**PAPER NUMBER**
2653	

DATE MAILED: 08/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/748,509	HAYASHI ET AL.	
	Examiner	Art Unit	
	Kim-Kwok CHU	2653	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-9* is/are rejected.

7)☒ Claim(s) *6 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

2. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Willis (U.S. Patent 6,693,857) in view of Arataki et al. (U.S. Patent 5,831,955).

Willis teaches a data buffer management controller for controlling interruption and restarting of data writing to a recording medium very similar to the instant invention. For example, Willis teaches the following:

(a) as in claim 1, a data recording medium 102 (Fig. 1);

(b) as in claim 1, a buffer memory 152 for temporarily storing data before data written to the recording medium 102 (Fig. 1; recording medium 102 is used record video/audio programs);

(c) as in claim 1, an encoder 150 connected to the buffer memory 152 (Fig. 1; MUX 150 contains video and audio encoding means);

(d) as in claim 1, the encoder 150 receives data to be written to the recording medium 102 and generates encoded data (Fig. 1; data such as video/audio programs are to be encoded and written to the recording medium 102);

(e) as in claim 1, a synchronizing circuit 134 for synchronizing the written data read from recording medium 102 with the encoded data when the writing of data to the recording medium 102 is interrupted (Fig. 1; buffer management; column 8, lines 37-49; column 8, lines 61-67);

(f) as in claim 1, a first retry determination circuit for determining whether an address of the write data, which read from the recording medium 102, and an address of the read data, which provided to encode, match (Figs. 1 and 3; matching address of a write data and a read data is a process of recording the data into a proper track address which is provided by the encoding means);

(g) as in claim 1, a second retry determining circuit for determining whether a timing (bit rate) for reading the write data from recording medium and a timing (bit rate) for encoding the read data match (Figs. 1 and 3; matching timing of a write data and a read data is a process of recording the data with a proper bit rate which is provided by the encoding means);

(h) as in claim 1, a restart circuit for restarting the writing of data to the recording medium based on the determining

of the first and second retry determination circuits (Figs. 1 and 3; restart is the recording data into a track and then another track in simultaneously read and write mode); and

(i) as in claim 2, the second retry determination circuit determines whether the timings match when the first retry determination circuit determines that the addresses match (Figs. 1 and 3; matching address and timing/bit rate of reading and writing data).

However, Willis does not teach the following:

(a) as in claim 1, the encoder receives data read from the buffer memory.

Arataki teaches an information recording system having an encoder 135 which receives data read from a buffer 123 (Fig. 3).

Input data such as video and audio requires a storage area as a waiting means so that it can be encoded according to a certain bit rate. Although Willis discloses a buffer means after an encoder, however, it would have been obvious to one of ordinary skill in the art to add a buffer means such as Arataki's in front of Willis's encoder means, because the buffer can be used as a temporary storage for the input data waiting to be encoded.

3. Claims 3-5 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Willis (U.S. Patent 6,693,857) in view of Arataki et al. (U.S. Patent 5,831,955).

Willis teaches a data buffer management controller for controlling interruption and restarting of data writing to a recording medium very similar to the instant invention. For example, Willis teaches the following:

(a) as in claim 3, a data recorder medium 102 (Fig. 1);

(b) as in claim 3, a buffer memory 152 for temporarily storing data before written to the recording medium 102 (Fig. 1);

(c) as in claim 3, an encoder 150 connected to the to the buffer memory 152 (Fig. 1; MUX 150 contains video and audio encoding means);

(d) as in claim 3, the encoder receives data read from the buffer memory and encodes the read data to generate encoded data (Fig. 1; data such as video/audio programs are to be encoded and written to the recording medium 102);

(g) as in claim 3, a synchronizing circuit for synchronizing written data medium with the encoded data (Fig. 1; buffer management; column 8, lines 37-49; column 8, lines 61-67);

(h) as in claim 3, a first retry determination circuit 134 for determining whether an address of the written data, which is read from the recording medium, and the write data address, which is stored in the one more address memories, match, (Figs. 1 and

3; matching address of a write data and a read data is a process of recording the data into a proper track address which is provided by the encoding means);

(i) as in claim 3, the first retry determination circuit 134 for determining whether an address of the read data, which is provided to the encoder from the buffer memory, and read data address, which is stored the one or more address memories, match Figs. 1 and 3; matching address of a write data and a read data is a process of recording the data into a proper track address which is provided by the encoding means);

(j) as in claim 3, a second retry determination circuit 134 determining whether a timing for reading the write data from the recording medium and a timing for encoding the read data match (Figs. 1 and 3; matching timing of a write data and a read data is a process of recording the data with a proper bit rate which is provided by the encoding means); and

(k) as in claim 3, a restart circuit restarting the writing data the recording medium based on the determinations of the first and second retry determination circuits (Figs. 1 and 3; restart is the recording data into a track and then another track in simultaneously read and write mode);

(l) as in claim 5, the second retry determination circuit determines whether the timings match when the first retry determination circuit determines that the addresses match (Figs.

1 and 3; matching timing (synchronization) and address of a write data and a read data is required in a recording/reading data operation);

However, Willis does not teach the following:

(a) as in claim 3, the encoder receives data read from the buffer memory;

(b) as in claim 3, one or more address memories connected to the buffer memory;

(c) as in claim 3, one more address memories store write data address of the data written to the recording medium and a read data address of the data read from the buffer memory when the writing of data to the recording medium is interrupted;

(d) as in claim 3, the write data address and the read data address each indicate a location of the data when the interruption occurs;

(e) as in claim 4, the written data read from the recording medium includes a first subcode synchronizing signal and the encoded data includes a second subcode synchronizing signal;

(f) as in claim 4, the second retry determination circuit determines whether the timing for reading the written data from the recording medium and the timing for encoding read data match based the first and second subcode synchronizing signals.

Arataki teaches an information recording system having the following features:

(a) an encoder 135 which receives data read from a buffer memory 123 (Fig. 3);

(b) as in claim 3, one or more address memories connected to the buffer memory 123 (Fig. 3; address memories are storage areas in the buffer memory 123; column 5; lines 5-10);

(c) as in claim 3, the address memories store write data address of the data written to the recording medium and a read data address of the data read from the buffer memory when the writing of data to the recording medium is interrupted (Fig. 3; address generator 124 generates read/write address which are stored in the buffer memory 123);

(e) as in claim 3, the write data address and the read data address each indicate a location of the data when the interruption occurs (Fig. 3; at any time including an interruption of the recording/reproducing operation, data stored in the buffer memory always attached with an address);

(f) as in claim 4, the written data read from the recording medium includes a first subcode synchronizing signal and the encoded data includes a second subcode synchronizing signal (column 11, lines 53-69; data before read has a subcode and data after encoded has a subcode; a subcode is a header attached to the data for synchronize read/write operations;

(g) as in claim 4, the second retry determination circuit determines whether the timing for reading the written data from

the recording medium and the timing for encoding read data match based the first and second subcode synchronizing signals (subcode needed to be match for proper read/write timing).

Input data such as video and audio requires a storage area as a waiting means so that it can be encoded according to a certain bit rate. Although Willis discloses a buffer means after an encoder, however, it would have been obvious to one of ordinary skill in the art to add a buffer means such as Arataki's in front of Willis's encoder means, because the buffer can be used as a temporary storage for the input data waiting to be encoded.

Furthermore, since data to be written or read are stored in the buffer memory first, to assign their addresses, it would have been obvious to one of ordinary skill in the art to use the buffer memory to store the read/write addresses of the data such as Arataki's, because data require their respective addresses so that they can be encoded/decoded properly.

4. Claims 7-9 have limitations similar to those treated in the above rejection, and are met by the references as discussed above.

Allowable Subject Matter

5. Claims 6 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

As in claims 6 and 10, the prior art of record fails to teach or fairly suggest the following features:

(a) a first location detection circuit connected to the one or more address memories, wherein the first location detection circuit detects whether the address of the written data read from the recording medium matches the write data address stored in the one of more address memories; and

(b) a second location detection circuit connected to the one or more address memories, wherein the second location detection circuit detects whether the address of the data read from the buffer memory matches the read data address stored in the one or more address memories.

The features indicated above, in combination with the other elements of the claims, are not anticipated by, nor made obvious over the prior art of record.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tsukihashi (6,584,053) is pertinent because Tsukihashi teaches an information recording/reproducing synchronizing means.

Maeda (6,272,084) is pertinent because Maeda teaches an information recording/reproducing having an interruption mode.

Kuroda et al. (6,219,309) is pertinent because Kuroda teaches an information recording/reproducing having an operation resume step.

Ishida et al. (5,680,379) is pertinent because Ishida teaches an information recording/reproducing synchronizing method.

Honda (5,586,093) is pertinent because Honda teaches an information recording/reproducing system having a buffer memory for storing suspended writing data.

8. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks Washington, D.C. 20231 Or faxed to:

(703) 872-9306 (for formal communications intended for entry. Or:

(703) 746-6909, (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2021 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-4700.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim CHU whose telephone number is (703) 305-3032.

KC 7/23/04

Kim-kwok CHU
Examiner AU2653
July 23, 2004

(703) 305-3032

William Korzuch
WILLIAM KORZUCH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600